Fabrication and Transfer of Flexible Few-Layers MoS_2 Thin Film Transistors to Any Arbitrary Substrate

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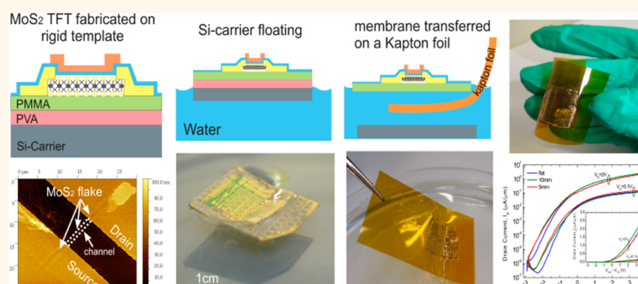
ABSTRACT Recently, transition metal dichalcogenides (TMDCs) have attracted interest thanks to their large field effective mobility (>100 $cm^2/V \cdot s$), sizable band gap (around 1−2 eV), and mechanical properties, which make them suitable for high performance and flexible electronics. In this paper, we present a process scheme enabling the fabrication and transfer of few-layers MoS_2 thin film transistors from a silicon template to any arbitrary organic or inorganic and flexible or rigid substrate or support. The two-dimensional semiconductor is mechanically exfoliated from a bulk crystal on a silicon/polyvinyl alcohol (PVA)/polymethyl methacrylane (PMMA) stack optimized to ensure high contrast for the identification of subnanometer thick flakes. Thin film transistors (TFTs) with structured source/drain and gate electrodes are fabricated following a designed procedure including steps of UV lithography, wet etching, and atomic layer deposited (ALD) dielectric. Successively, after the dissolution of the PVA sacrificial layer in water, the PMMA film, with the devices on top, can be transferred to another substrate of choice. Here, we transferred the devices on a polyimide plastic foil and studied the performance when tensile strain is applied parallel to the TFT channel. We measured an electron field effective mobility of 19 $cm^2/(V\ s)$, an I_{on}/I_{off} ratio greater than 10^6, a gate leakage current as low as 0.3 pA/μm, and a subthreshold swing of about 250 mV/dec. The devices continue to work when bent to a radius of 5 mm and after 10 consecutive bending cycles. The proposed fabrication strategy can be extended to any kind of 2D materials and enable the realization of electronic circuits and optical devices easily transferrable to any other support.



KEYWORDS: MoS_2 · flexible electronics · graphene · transition metal dichalcogenides · mobility · bending radius · transfer technique

The development of high speed and low power circuits on mechanically flexible substrates may enable new applications in electronics, sensing, and energy.[1−7] Over the last decades, great progress in the printing and transfer of single-crystalline, inorganic micro- and nanostructures on plastic substrates has been achieved through various process schemes.[3,8−13] However, combining large scale integration and high performance remains still challenging and the quest for high mobility and low temperature processable materials is very actual. Recently, the advances in processing graphene sheets[14] has renewed the interest of the scientific community for two-dimensional materials and their remarkable electronic and optical attributes.[15,16] These materials can stand high mechanical strain thanks to their strong in-plane bonding; at the same time, their only few-atomic layer thickness provides high flexibility. In addition, chemical vapor deposition (CVD) growth[17,18] could lead to large area integration. This class of 2D materials provides also a complete set of electronic properties ranging from metal-like behavior (graphene), semiconductors (transition metal dichalcogenides (TMDCs)), to dielectrics with a large band gap (like boron nitride (BN)). Charge carrier in graphene can display an exceptionally high mobility exceeding 10^5 $cm^2/(V\ s)$ at room temperature;[19] however, graphene lacks an intrinsic band gap and field-effect transistors made from graphene cannot be effectively switched off and have low on/off switching ratios. In contrast, several 2D

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TMDCs, such as MoS_2, $MoSe_2$, WS_2, and WSe_2, possess an intrinsic and sizable band gap of around 1−2 eV[20,21] and charge carriers mobility larger than 100 $cm^2/(V s)$,[22−24] allowing applications such as transistors, photodetectors, and electroluminescent devices. Mechanical measurements performed on single-layer MoS_2 show that it is 30 times as strong as steel and can be deformed up to 11% before breaking,[25] which makes this material one of the strongest and most resilient semiconducting materials advantageous for flexible substrates. After the demonstration of a 200 $cm^2/(V s)$ mobility for a single-layer MoS_2 transistor with high-K dielectric[22] in 2011, much work has been focused mostly on rigid substrates.[23,26−28] Few results have been shown on flexible substrates,[29−31] despite the fact that high-performance flexible electronics remain one of the most promising applications.[32] Reproduced on plastic, the same performance measured on silicon is challenging because of the difficulties in combining low temperature processing, high-K dielectric integration, and high quality TMDCs materials. Recently, Chang *et al.* reported flexible MoS_2 TFTs with high-K dielectric showing a mobility as high as 30 $cm^2/(V s)$ and excellent mechanical stability.[31] To date, however, there is no designed and reproducible procedure enabling the microfabrication of few-layers TMDCs transistors on flexible substrate with high-K dielectric and structured source, drain, and gate metallic contacts, indispensable for the fabrication of electronic circuits.

In this paper, we present a process scheme which allows the identification of mechanically exfoliated single or few-layer thick MoS_2 flakes on a Si/PVA/PMMA substrate and the microfabrication of thin film transistors with high-K dielectric and structured source, drain, and gate electrodes. The devices are fully fabricated on the aforementioned substrate and can be transferred to any destination support after the dissolution of the PVA sacrificial layer in water and the release of the PMMA membrane. Here, we transferred the TFTs onto a 50 μm thick polyimide substrate and characterized them in the flat condition, when bent to 10 mm and 5 mm radius and after 10 consecutive bending cycles. The devices show an electron field effective mobility of 19 $cm^2/(V s)$, an I_{on}/I_{off} ratio greater than 10^6, a gate leakage current as low as 0.3 pA/μm, and a subthreshold swing of about 250 mV/dec.

RESULTS AND DISCUSSION

Mechanical exfoliation through an adhesive tape technique is an easy and fast way to produce thin and good quality flakes of two-dimensional layered materials[16] processable with standard lithography techniques. Similar to the pioneer work of C. R. Dean,[33] we exfoliated MoS_2 flakes on top of a Si/PVA/PMMA substrate in order to successively dissolve the PVA layer in water and mechanically transfer the PMMA membrane onto the destination substrate. A good optical contrast is important to easily identify and locate, at the optical microscope, single or few-layer thick flakes. By using a model based on the Fresnel's law,[34] we investigated the dependence of the contrast on the PMMA thickness while keeping the PVA

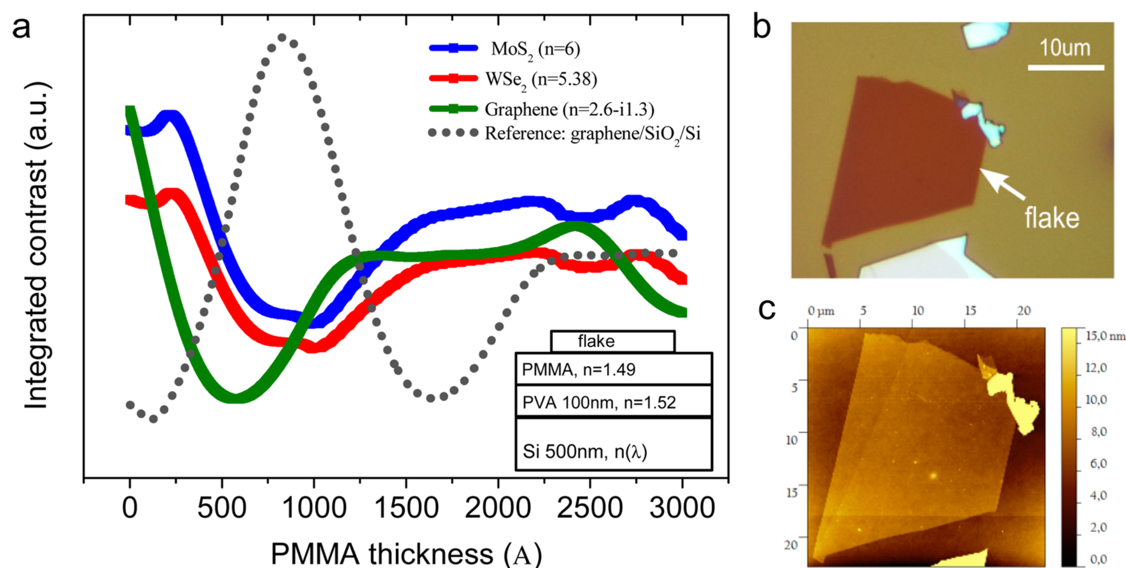

Figure 1. (a) Contrast dependence on the PMMA thickness for MoS_2, WSe_2 and graphene. The calculation is based on Fresnel's law and the contrast is integrated over the wavelength range 400−800 nm assuming white light illumination and no optical filters. The template consists of a semi-infinite silicon layer whose refractive index is wavelength-dependent, a PVA layer of 100 nm with $n = 1.52$, and the PMMA film with $n = 1.49$. MoS_2, WSe_2, and graphene have $n = 6, 5$, and 2.6-i1.3, respectively. An optimal thickness of 200 nm is chosen for the PMMA film. The calculation is validated in the case of graphene/SiO_2/Si template with the oxide thickness as variable (SiO_2 is modeled with a refractive index of 1.46[34]). The curve shows the well-known peaks at 90 and 285 nm. (b) Optical microscope picture of a 10×15 μm^2 large flake. (c) Atomic force microscopy (AFM) of the same flake shown in (b). The thickness is about 3.5 nm, corresponding to 5−6 atomic layers.

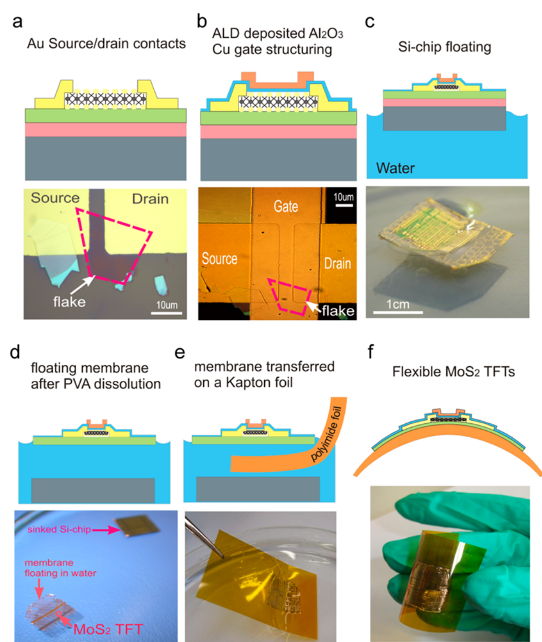

Figure 2. Process scheme for the fabrication of MoS_2 thin film transistors. (a) After the identification of the flake (same as Figure 1b,c), source/drain contacts are formed by evaporation of a 100 nm Au thin film, UV-lithography patterning, and $K_2 + I_2$ wet etching. (b) Al_2O_3 (25 nm) and 50 nm of e-beam evaporated Cu forms the gate dielectric and the gate contact, respectively. (c) After the device fabrication, the chip is made to float in water to release the top PMMA membrane after the dissolution of the PVA film. (d) After 10 min (for a 2 × 2 cm^2 chip), the PMMA membrane is floating in water, while the chip sinks to the bottom of the beaker. (e) The membrane, with the MoS_2 transistors on top, is transferred onto a polyimide foil acting as destination substrate. The foil is dipped into water in the proximity of the membrane and then lifted up. (f) The foil is then baked for 10 min at 70 °C to evaporate the remaining water and to improve the adhesion.

thickness constant (100 nm). We assumed a refractive index, n, of 1.52 and 1.49 for PVA and PMMA, respectively.[35,36] MoS_2 is modeled by n = 6 and a thickness, d, of 0.65 nm for a single layer.[37] The silicon layer, instead, has been considered semi-infinite, with a refractive index which is wavelength dependent.[34] The contrast was integrated over the visible spectrum (λ = 400−800 nm) under the hypothesis of white light illumination and the absence of any optical filter. We repeated the calculation for graphene (d = 0.34 nm, n = 2.6-i1.3)[34] and WSe_2 (d = 0.65 nm, n = 5.38),[38] which exhibits a p-type behavior,[24] hence, useful for complementary logic circuits if combined with MoS_2. Based on the results shown in Figure1a, we selected an optimum thickness of 200 nm for the PMMA film. In our experiments, flakes with thicknesses between 3.5 and 10 nm were selected by optical microscope and then characterized by atomic force microscopy (AFM). Figure 1b, c show an optical microscope picture and the corresponding AFM image of a 3.5 nm thick flake on the Si/PVA/PMMA chip.

After the identification of the flake, we deposited by electron beam evaporation a continuous 100 nm layer of Au and patterned it by UV-lithography for source/drain contacts areas definition (Figure 2a). The Au layer was etched by a $K_2 + I_2$ solution. To guarantee good electrical coupling between the gate and the transistor channel and to enhance screening effect and reduce Coulomb scattering,[22,39] we deposited 25 nm of Al_2O_3 ($\varepsilon_r \approx 9.5$) by atomic layer deposition (ALD) technique. The deposition temperature is 150 °C and it is also the maximum temperature achieved during the process. Top gate consists of 50 nm of e-beam evaporated Cu, which is patterned by UV lithography and wet etched by iron chloride hexahydrate solution (Figure 2b). After the completion of the device fabrication, the PVA layer is dissolved with water in order to release the PMMA membrane on top the TFTs (Figure 2c). For a 2 × 2 cm^2 chip, the release phase takes about 10 min, after which the PMMA layer is floating on water (Figure 2d). In this study, we transferred the PMMA thin film directly onto a 50 μm thick polyimide foil in order to study the electrical performance while bending (Figure 2e and Figure S1 in Supporting Information). The polyimide-membrane sample is baked at 70 °C for 10 min to evaporate the remaining water and was found to improve the adhesion between the two layers (Figure 2f).

After the transfer, we electrically characterized our devices in flat conditions. An example of the transfer and output characteristic and of C−V measurement is shown in Figure 3. The devices exhibit an I_{on}/I_{off} ratio greater than 10^6, with an off current as low as 0.3 pA/μm and a subthreshold swing of about 250 mV/dec. The use of Cu (work function about 4.65 eV) as metal for the top gate contact sets a negative threshold voltage of about −2 V. A non-optimum gate electrostatic control of the transport in the channel is responsible of the threshold shift observed in the I_D curve for low and high gate voltage. This is explained by the bad quality of MoS_2/oxide interface, which will be better analyzed later on. The relatively high value for the subthreshold swing and the hysteretic behavior in the transfer characteristic can also be ascribed to the same cause. Through the $I_D/\sqrt{g_m}$ method[40] we extracted a field effect mobility of about 19 $cm^2/(V\ s)$ (see Figure S2 in Supporting Information). Such value is in good agreement with previously reported works on flexible substrate[30,31] and with nonencapsulated structures.[22] Double gate architecture with high-K gate dielectric could reveal higher mobility and reproduce, on plastic, the performance already demonstrated in similar structures on rigid substrate.[22,23] Gold source and drain contacts show a linear-like behavior (see Figure S3 in Supporting Information), however, the use of low work-function materials[23] for source/drain contacts could further reduce the contact resistance. The I_D-V_{DS} curves show a saturating behavior, and the output resistance, $1/g_{DS}$, is about 1.5 MΩ at $V_D = V_{GS} = 2$ V for a TFT with channel width/length of 10 μm/4.3 μm (Figures 3b and S4 in

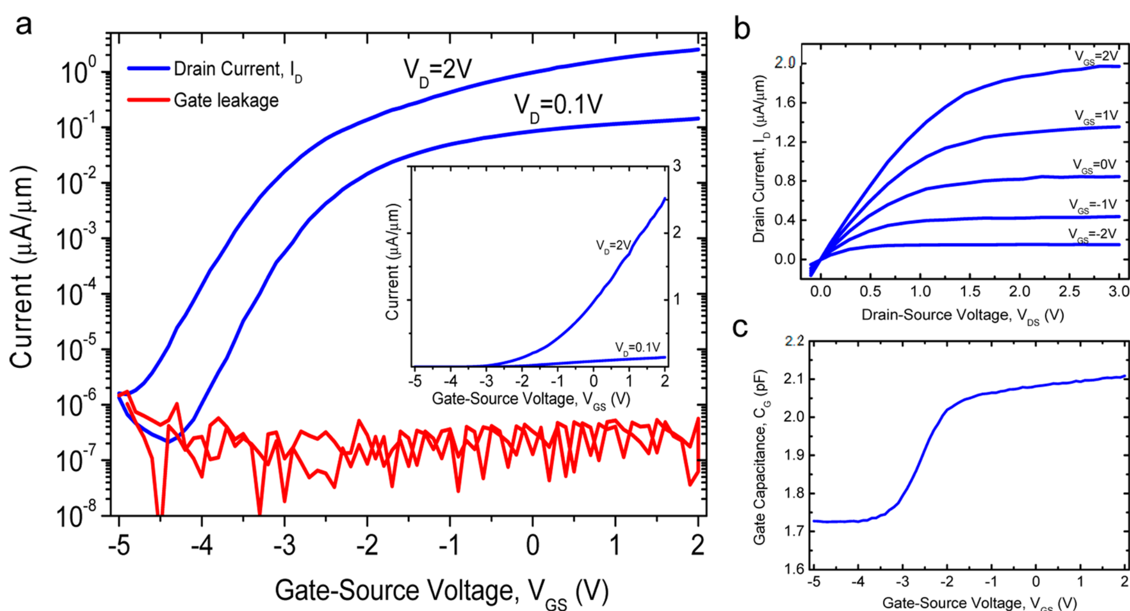

Figure 3. Electrical characterization of a MoS_2 transistor on a polyimide foil. The measurements have been performed in flat condition and refer to the 3.5 nm flake of Figure 1b,c. (a) Transfer characteristic of a transistor with a channel length and width of 4.3 and 10 μm, respectively. The device shows a mobility of 19 cm^2, a I_{on}/I_{off} greater than 10^6, and a subthreshold slope of 250 mV. The threshold voltage is about −2 V. The shift of the I_d-V_g curve for low and high V_D could be explained by charge traps present at the MoS_2/oxide interface. The inset shows the same curves in linear scale. (b) Output characteristic of the same device. The curves show a saturating behavior and the calculated output resistance for $V_D = V_{GS} = 2$ V is about 1.5 MΩ. (c) Capacitance−voltage measurements performed with source and drain grounded at a frequency of 1 MHz.

Supporting Information). For the same device, the intrinsic gain g_m/g_{DS}, where g_m is the transconductance $\partial I_D/\partial V_{GS}$, is about 16 at $V_D = V_{GS} = 2$ V (see Figure S4 in Supporting Information).

To understand the origin of the aforementioned poor MoS_2/oxide interface, we have studied the surface of the channel region by atomic force microscopy (AFM) in tapping mode before and after the source/drain gold deposition and etching. The AFM images (see Figure 4) highlight a rougher surface of the MoS_2 after contacts deposition and etching if compared to the preprocessed flake surface. Process residues lying on top of the channel can be seen in the AFM images (see Figure 4e). They could be the origin of interface trap charges which could affect the device electronic properties and impact on the poor subthreshold swing and hysteretic behavior observed in the transfer characteristic. Similar effects are observed in graphene transistors.[41,42] It is worth mentioning that lift-off, acetone cleaning, O_2 plasma, or Ar/H_2 annealing cannot be used in our process scheme because of the fragile PMMA layer. The optimization of the Au etching could lead to a cleaner surface.

The interface charge density can be extracted through a very simple model. In fact, the subthreshold swing of a transistor can be written as[43,44]

$$SS = \frac{K_B T}{q} \ln 10 \left(1 + \frac{C_S}{C_{OX}} + \frac{C_{IT}}{C_{OX}}\right) \quad (1)$$

where K_B is the Boltzmann constant, T is the temperature, q is the electron charge, C_S, C_{OX}, and C_{IT} are the semiconductor, the dielectric, and the interface charge capacitances, respectively. Under the hypothesis of an ideal interface ($C_{IT} = 0$) and of a perfect gate-channel coupling ($C_S/C_{OX} \approx 0$), which is usually the case in ultrathin body transistors, the subthreshold swing reaches the ideal value of 60 mV/dec. Taking such values as reference, we found a C_{IT} of about 10.2×10^{-7} F/cm^2 and a density of charge $D_{IT} = 6.4 \times 10^{12}$ cm^{-2} (see Supporting Information for more details).

To study the flexibility of the TFTs on the polyimide substrate, we bent the devices around rods (Figure S5 in Supporting Information) with a radius of 10 and 5 mm, corresponding to a strain level of 0.3% and 0.5% respectively, in a way that tensile strain is applied parallel to the TFT channel. Subthreshold swing, mobility, and I_D current levels remain almost constant, as is also shown in other works[30,31] (Figure 5a). The I_{on}/I_{off} ratio remains greater than 10^5, with an I_{off} current smaller than 1 pA/μm, while gate leakage is as low as 0.3 pA/μm for the full range of operations. We also observed a gradual threshold voltage shift toward left when strain is applied, as shown in the $C-V$ measurements of Figure 5b. In particular, for the device of Figure 3, we extracted, through the Ghibaudo's method,[40] values of −2.12, −2.18, and −2.23 V for flat, 10 mm, and 5 mm bending radii, respectively (see Figure S6a in Supporting Information, which shows the output characteristic).

To evaluate the influence of multiple bending, the flexible transistors were characterized before and after 10 cycles at 10 mm as minimum bending radius (see Figure S5 in Supporting Information). We noticed a

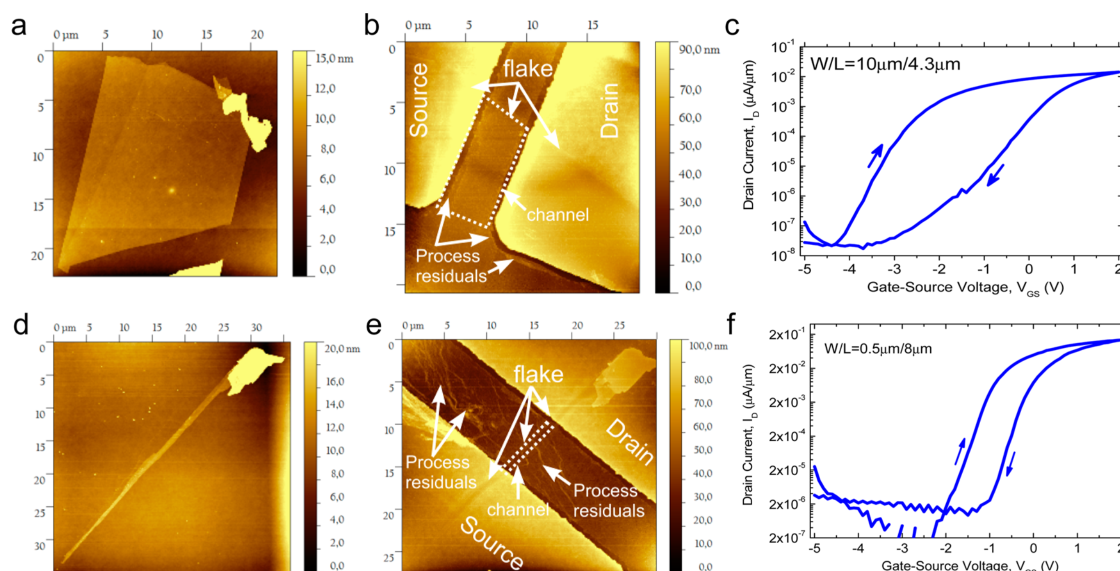

Figure 4. Two examples of atomic force microscopy (AFM) surface analysis of the channel area before and after the Au source/drain structuring. (a, d) Flakes before the Au deposition exhibits an average surface roughness of about 0.3 nm. (b, e) Flakes after the Au deposition and etching shows an average surface roughness greater than 4–5 nm. Process residuals are clearly visible in the AFM images. (c, f) Hystheretic behavior of the transfer characteristic (V_D = 0.1 V) for TFTs corresponding to flake in (b, e). The hysteresis as well as the large subthreshold swing is thus explained by interface trap charges present at the MoS_2/oxide interface.

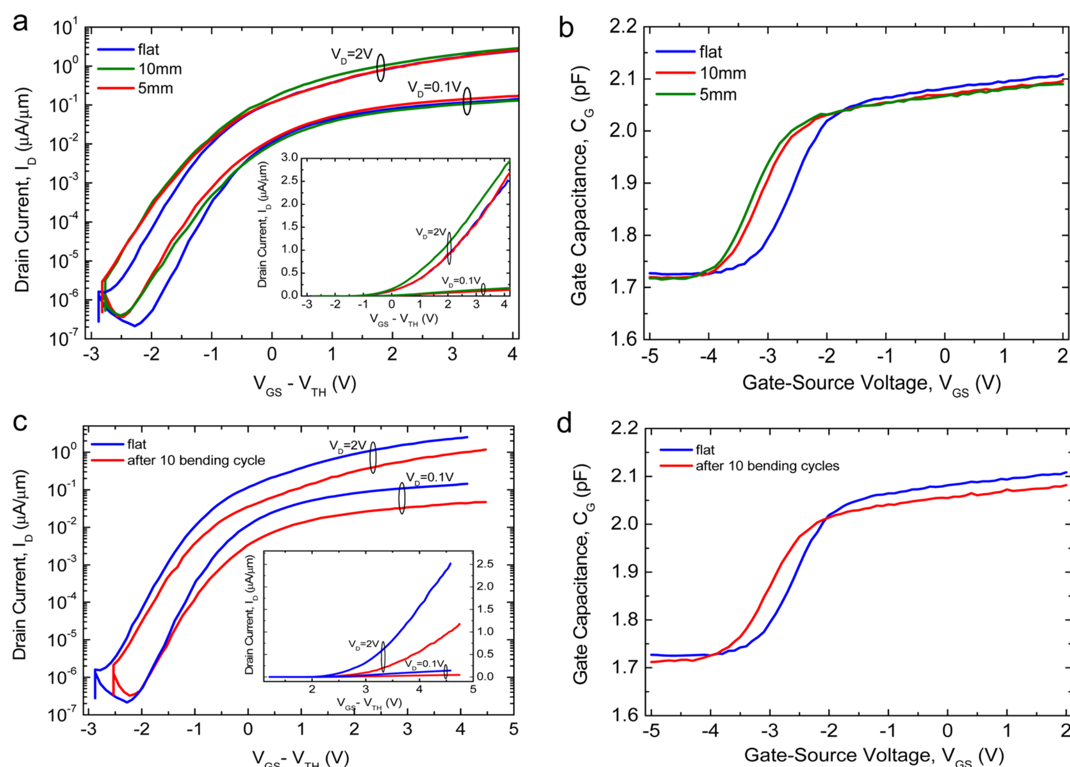

Figure 5. Electrical performance of a flexible MoS_2 transistor under strain. The device is the same as Figure 3. (a) Drain current plotted against the gate overdrive, $V_{GS}-V_{TH}$, shows a slight increase when the device is bent to 10 and 5 mm. (b) $C-V$ measurements show a shift of the threshold voltage toward left, while the capacitance levels remain almost unaltered for all regions of the operation (depletion, weak and strong inversion). (c) Transfer characteristics of the device after 10 consecutive bending cycles at 10 mm bending radius. We observed a decrease of a factor 1/2 of the current level in strong inversion compared to flat condition. (d) $C-V$ measurement before and after 10 bending cycles. A shift of the threshold voltage toward left confirms the behavior observed in (b). We noticed also a decrease of 2.5% of the capacitance level in strong inversion. Hence, the deterioration of the drain current in strong inversion highlighted in (c) is mostly explained by conduction mechanism and not by a dielectric degradation.

deterioration of the performance in terms of current levels. The drain current in strong inversion decreased of a factor 1/2 (see the I_D-V_{GS} plot in linear scale in Figure 5c) if compared to the curves in the flat condition (see also Supporting Information for the output characteristic). This mechanism is explained by a degradation of the transistor conduction mechanisms, hence, by an increase of the source/drain contact resistance or by the deterioration of the semiconductor mobility. In fact, the ALD dielectric properties remain unaltered as is visible from the gate capacitance, which decreased only by 2.5% in strong inversion (Figure 5d). This effect is mirrored by a decrease of the I_{on}/I_{off} ratio. A shift of the threshold voltage toward left of about 350 mV and a subthreshold swing deterioration is also observed. Gate leakage and I_{off} current remained almost unchanged. The devices do not withstand a long cycling test (<20 cycles). The poor robustness could be due to the large interface charge density, which could play a role in long time fatigue test, contacts degradation, and cracks across the flakes.

CONCLUSIONS

In conclusion, we have shown a universal process scheme to fabricate MoS_2 thin film transistors on a carrier template and then transfer them onto potentially any type of substrate material. The devices are fully fabricated on a silicon/PVA/PMMA chip and consist of top gate architecture with Au source and drain, Al_2O_3 dielectric, and Cu gate electrode. After the completion of the fabrication, PVA is dissolved in water and the PMMA film is released. As first demonstration, we transferred the TFTs onto a polyimide foil and studied the performance while bending. We measured a mobility of 19 $cm^2/(V\ s)$, an I_{on}/I_{off} ratio greater than 10^6, and a threshold voltage of about -2 V. The observed hysteretic behavior of the transfer characteristic is explained by the presence of trap charges at the MoS_2/oxide interface after etching of source and drain contacts. The devices continue to work with almost unchanged performance when bent down to a 5 mm bending radius. After 10 consecutive bending cycles, we noticed a decrease of the current in strong inversion, which we explained by channel conduction deterioration rather than oxide degradation. The proposed fabrication strategy can be extended to any kind of 2D materials and could enable the realization of electronic circuits and optical devices easily transferrable to any other support like flexible substrate.

MATERIAL AND METHODS

Contrast Calculation. The contrast has been calculated similarly to the method reported for graphene,[34] with the only difference that it has been integrated over the visible spectrum under the assumption of white light illumination. To validate the method, we calculated the contrast for a Si/SiO_2 template in the case of a graphene single layer and we obtained the two known peaks at 90 and 285 nm as SiO_2 thickness.

Device Fabrication. The Si/PVA/PMMA substrate was prepared by spin coating 100 nm of PVA (Sigma Aldrich) and 200 nm of PMMA (495k molecular weight from Micro-Chem) both at 4000 rpm for 50 s. MoS_2 devices were mechanically exfoliated from commercial crystals (SPI supplies). Source/drain were formed by electron-beam evaporating of 100 nm Au layer, defined by standard UV lithography using AZ1518 positive resist and etched by $K_2 + I_2$ solution. The option of using a thin layer of chromium as adhesion layer has been evaluated but because of the difficulties in etching the layer we noticed short circuits between source and drain contacts. The gate dielectric consists of 25 nm of Al_2O_3 deposited by ALD at 150 °C. Gate contact is an evaporated 50 nm layer of Cu which is patterned by UV-lithography and etched by a by iron chloride hexahydrate solution. The resist removal is performed by a blank exposure and by a subsequent development step (Microprosit developer). The devices are fully fabricated on the Si/PVA/PMMA substrate and then placed in water to release the PMMA membrane after the dissolution of the PVA layer. The release phase takes about 10 min in the case of a $2 \times 2\ cm^2$ chip and can be facilitated by smoothly and carefully scratching the edges of the chip. The floating PMMA membrane is transferred onto a 50 μm polyimide foil which is dipped in water and then lifted up in proximity of the PMMA layer. The polyimide$-$PMMA membrane is baked at 70 °C for 10 min in order to evaporate the remaining water and to improve the adhesion.

Devices Characterization. Asylum AFM was used to characterize the thickness and surface of the MoS_2 flakes. The roughness analysis has been performed by the Gwyddion software. Electrical characterization is performed by HP analyzer. Capacitance measurements are performed at 1 MHz after proper calibration. The measurements under bent condition are done by attaching the devices around a metallic rod of the desired radius with a double-side scotch tape Bending cycles are performed by placing the device in a home-built machine that bends the foil to a 10 mm bending radius.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Picture of the membrane after the transfer on the polyimide substrate, the I_D-V_D at low voltage, the mobility extraction method, the g_m, g_{DS}, and intrinsic gain, the g_m/I_D and g_m/C plots, a description of the bending tests and the corresponding output characteristics. This material is available free of charge *via* the Internet at http://pubs.acs.org

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